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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,725	03/21/2006	Seon Ho Han	CU-4700 WWP	6890

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EXAMINER	
HSIEH, PING Y	

ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,725	HAN ET AL.	
	Examiner	Art Unit	
	PING Y. HSIEH	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 1/29/09 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,432,768 has been reviewed and is accepted. The terminal disclaimer has been recorded.

2. In view of the terminal disclaimer filed on 1/29/09, the double patenting rejection is withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-15 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al. (U.S. PATENT NO. 7,089,032) in view of Oono et al. (U.S. PATENT NO. 7,085,587), Kim et al. (U.S. PG-PUB NO. 2004/0048591) and further in view of Welland et al. (U.S. PG-PUB NO. 2003/0119467).

-Regarding claims 1, 3, 8 and 13, Hongo et al. disclose an RF front-end transceiver **(as disclosed in fig. 2)** comprising: an oscillator for outputting a resonant frequency signal whose frequency is controlled by a frequency control signal **(frequency synthesizer part 140 and 141 as disclosed in fig. 2 and further disclosed in col. 7 lines 6-10)**; a receive amplifier for amplifying and

outputting a receive RF signal **(amplifier 122 as disclosed in fig. 2 and further disclosed in col. 7 lines 59-63)**; a receive mixer for mixing the receive RF signal amplified and the resonant frequency signal **(mixer 123 as disclosed in fig. 2 and further disclosed in col. 7 lines 59-63)**; a transmit mixer for mixing a transmit base band signal and the resonant frequency signal to convert the transmit base band signal into a transmit RF signal **(mixer 112 as disclosed in fig. 2 and further disclosed in col. 7 lines 3-6)**; and a transmit amplifier for amplifying and outputting the transmit RF signal **(amplifier 130 as disclosed in fig. 2 and further disclosed in col. 7 lines 3-6)**, wherein a resonant frequency of at least one of the receive amplifier, the receive mixer, the transmit mixer and the transmit amplifier is controlled by the frequency control signal **(frequency synthesizer part 140 and 141 generates a number of frequencies by their switching to effectively share frequency channels assigned to a system as disclosed in fig. 2 and further disclosed in col. 7 lines 6-9)**. However, Hongo et al. fail to disclose the receive mixer converts the receive RF signal into a receive base band signal.

Oono et al. disclose a direct conversion system for directly down-converting a received signal to a baseband signal (I/Q) as disclosed in col. 1 lines 39-53.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the mixer as disclosed by Hongo et al. to be able

to direct convert the received signal to a baseband signal as disclosed by Oono et al. One is motivated as such in order to reduce the circuit size.

However, the combination fails to specifically disclose a frequency synthesizer providing a frequency control signal; such that frequency of the oscillator, receive amplifier, receive mixer, transmit mixer, transmit amplifier are controlled by the frequency control signal.

Kim et al. disclose a frequency synthesizer includes a PLL as disclosed in paragraph 47; and a control voltage from the phase locked loop (PLL) controls VCO, amplifier and mixer as disclosed in fig. 1A and 1B and abstract.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the PLL of Hongo et al. to be replaced with the PLL as disclosed by Kim et al., so the PLL can control the frequency of the oscillator, receive amplifier, receive mixer, transmit mixer, transmit amplifier. One is motivated as such in order to reduce the number of required components in the multiband RF transceiver.

The combination further discloses the frequency synthesizer comprises a phase frequency detector for receiving a reference frequency f_{REF} **(Kim et al., phase detector 340, fig. 3)**; a low pass filter **(Kim et al., loop filter 350 includes a low pass filter as disclosed in fig. 3 and paragraph 48)**; the oscillator operatively coupled to the LPF, wherein the oscillator providing the output resonant frequency, f_{LO} **(Kim et al., VCO 360 as disclosed in fig. 3 and paragraphs 47-51)**; an N divider operatively coupled to the DAT-VCO and to the

PFD **(Kim et al., N divider 330 as disclosed in fig. 3)**. However, the combination fails to specifically disclose a current pump operatively coupled to the phase frequency detector; a low pass filter operatively coupled to the current pump; a digital tuner in parallel to the low pass filter and operatively coupled to the current pump; and the oscillator operatively coupled to the LPF and to the DT, wherein the oscillator is a digital analog tuning voltage controlled oscillator for providing the output resonant frequency, f_{LO},; and the frequency control signal is VAT and VDT signals.

Welland et al. disclose a current pump operatively coupled to the phase frequency detector **(CP 208 is coupled to PD 206 as disclosed in fig. 5)**; a low pass filter operatively coupled to the current pump **(LF 210 is coupled to CP 208 as disclosed in fig. 5)**; a digital tuner in parallel to the low pass filter and operatively coupled to the current pump **(discrete control 502 is in parallel with LF 210 and coupled to CP 208 as disclosed in fig. 5)**; the oscillator operatively coupled to the LPF and to the DT **(VCO 400 is coupled to LF 210 and discrete control 502 as disclosed in fig. 5)**, wherein the oscillator is a digital analog tuning voltage controlled oscillator for providing the output resonant frequency, f_{LO} **(VCO 400 is a digital analog VCO as disclosed in fig. 5 and further disclosed in paragraph 56-60)**; and VCO is controlled by VAT and VDT signals **(Vc and Bc signals as disclosed in fig. 5)**.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the PLL to include the frequency synthesizer as

disclosed by Welland et al. One is motivated as such in order to integrate the VCO with the other components of the PLL onto a single integrated circuit for size consideration.

-Regarding claims 2, 4, 9 and 14, the combination further discloses the VAT and VDT signals are provided from the base band processor **(Hongo et al., frequency synthesizer part 140 and 141 as disclosed in fig. 2 and further disclosed in col. 7 lines 6-10; Welland, Vc and Bc signals as disclosed in fig. 5)**.

-Regarding claims 5, 10, 15, 17 and 20, although the combination does not specifically disclose the receive amplifier has either a common gate amplifier configuration or a cascode amplifier configuration, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the amplifier configuration to be either common gate or cascode since both configuration are basic configurations of electronics amplifiers.

-Regarding claims 6, 11, the combination further discloses the frequency of the f_{Lo} is controlled by VAT and VDT signals, and wherein, a resonant frequency of the receive amplifier and the receive mixer is controlled by the VAT and VDT signals **(Hongo et al., frequency synthesizer part 140 and 141 as disclosed in fig. 2 and further disclosed in col. 7 lines 6-10; Welland et al., fig. 5)**.

-Regarding claims 7, 12 and 18, the combination further discloses the receive amplifier has a net input resistance controlled by the VAT and VDT signal

(Oono et al., the second stage amplifier PGA2 and the third stage PGA3 are respectively configured so as to be capable of adjusting input offsets with resistors attached to their input terminals as disclosed in col. 9 lines 28-47; Welland et al., as disclosed in fig. 5).

-Regarding claim 19, the combination of Hongo et al. and Oono et al. discloses all the limitation as claimed in claim 1. The combination further discloses a base band processor for inputting the receive base band signal and for outputting the transmit base band signal **(Oono et al., col. 1 lines 39-53)**, wherein the DAT-VCO, the receive amplifier and the receive mixer comprising an RF front-end receiver exhibiting an input impedance **(it is inherent for the oscillator, amplifier and mixer to have an input impedance)**; the transmit mixer and the transmit amplifier comprising an RF front-end transmitter exhibiting and having an output impedance **(it is inherent for the amplifier and mixer to have an output impedance)**; and the DAT-VCO, the receive amplifier, the receive mixer, the transmit mixer and the transmit amplifier are controlled by the VAT and VDT signals to substantially match an input impedance with an output impedance of the transceiver such that the transceiver transmits substantially a maximum power over a specific frequency band **(Impedance should be matched in designing the RF front-end transceiver in order to transmit maximum power as disclosed in applicant's admitted prior, paragraph 6 in the specification)**.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al. (U.S. PATENT NO. 7,089,032) in view of Oono et al. (U.S. PATENT NO. 7,085,587), Kim et al. (U.S. PG-PUB NO. 2004/0048591), Welland et al. (U.S. PG-PUB NO. 2003/0119467) and further in view of Van Rumpt (U.S. PATENT NO. 7,299,018).

-Regarding claim 16, the combination of Hongo et al. and Oono et al. discloses all the limitation as claimed in claim 13. However, the combination fails to specifically disclose a LC tank including a capacitor controlled by the VDT signal, a capacitor controlled by the VAT signal and a fixed capacitor.

Van Rumpt discloses a LC tank including a capacitor controlled by the digital frequency control signal, a capacitor controlled by the analog frequency control signal and a fixed capacitor **(as disclosed in fig. 1B and further disclosed in col. 5 line 31-col. 6 line 38)**.

Therefore, it would have been obvious to one of ordinary skills in the art at the time of invention to modify the oscillator as disclosed by Hongo et al. and Oono et al. to be the variable capacitance bank as disclosed by Van Rumpt. One is motivated as such in order to lower the bias voltage and to avoid the need for DC/DC converters.

Response to Arguments

6. Applicant's arguments filed 1/29/09 have been fully considered but they are not persuasive.

a. In pages 12-15 of the remarks, regarding claims 1, 3, 8 and 13, applicant argues that none of Hongo, Oono, Kim, Van Rumpt, or Welland discloses at a

frequency synthesizer or a base band processor having a phase frequency detector (PFD) as now required in independent claims 1, 3, 8 and 13.

-The examiner respectfully disagrees. Welland indeed discloses a frequency synthesizer 500 having a phase frequency detector 206 as disclosed in fig. 5 and paragraph 56. Therefore, other references do not need to teach it.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PING Y. HSIEH whose telephone number is (571)270-3011. The examiner can normally be reached on Monday-Thursday (alternate Fridays) 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lana N. Le can be reached on (571)272-7891. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/P. Y. H./
Examiner, Art Unit 2618

/Lana N. Le/
Primary Examiner, Art Unit 2614